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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,164	08/18/2003	Jonathan E. Greene	102323-0130	3585

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EXAMINER

DO, CHAT C

ART UNIT	PAPER NUMBER
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2193

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/643,164

Applicant(s)

GREENE, JONATHAN E.

Examiner

Chat C. Do

Art Unit

2193

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 19 May 2005 and 20 August 2004.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 47-57 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 47-49 and 51-57 is/are rejected.
- 7) ☒ Claim(s) 50 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

RD

### **DETAILED ACTION**

1. This communication is responsive to Amendment filed 05/19/2005 and 08/20/2004.
2. Claims 47-57 are pending in this application. Claims 47, 52, and 55 are independent claims. In Amendment, claims 1-46 are cancelled and claims 47-57 are added. This Office Action is made final.

#### ***Claim Objections***

3. Claim 51 is objected to because of the following informalities:

Re claim 51, the applicant is advised to re-write the term "SIMD" in full as "single instruction multiple data" in line 2.

Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 47, 52, and 55 are rejected under 35 U.S.C. 102(b) as being anticipated by Kozaki et al. (U.S. 6,058,409).

Re claim 47, Kozaki et al. disclose in Figures 6-7 a system for performing a fast Fourier transform on  $N$  ordered inputs in  $n$  stages (e.g. abstract and Figure 6) comprising: a non-final stage calculating means for repetitively performing in-place butterfly calculations for  $n-1$  stages (e.g. 4 Figure 6); a final stage calculating means (e.g. last 4 and 6 in Figure 6) for performing a final stage of butterfly calculations including: a first loop means (e.g. last 4 and 6 in Figure 6 for computing  $F(0)$  and  $F(7)$ ) for performing a portion of the final stage butterfly calculations, the first loop means performing the set of butterfly calculations, and storing butterfly calculation outputs in shuffled order in place of the selected inputs to result in a correct ordering of transform outputs; and a second loop means (e.g. last 4 and 6 in Figure 6 for computing  $F(1)$  to  $F(6)$ ) for performing a remaining portion of the final stage butterfly calculations, the second loop means performing two sets of butterfly calculations, and storing butterfly calculation outputs from a first one of the two sets of butterfly calculations in shuffled order in place of the inputs selected for a second one of the two sets of butterfly calculations and storing butterfly calculation outputs from the second one of the two sets of butterfly calculations in shuffled order in place of the inputs selected for the first one of the two sets of butterfly calculations to result in a correct ordering of transform outputs (e.g. col. 8 lines 35-48).

Re claim 52, Kozaki et al. disclose in Figures 6-7 a method for performing a fast Fourier transform on  $N$  ordered inputs in  $n$  stages (e.g. abstract and Figure 6) comprising: performing non-final stage calculations by repetitively performing in-place butterfly calculations for  $n-1$  stages (e.g. 4 Figure 6); performing final stage calculations (e.g. last 4

and 6 in Figure 6) by performing a final stage of butterfly calculations in a first loop (e.g. last 4 and 6 in Figure 6 for computing F(0) and F(7)) for performing a portion of the final stage butterfly calculations and in a second loop for performing a remaining portion of the final stage butterfly calculations, wherein each of the butterfly calculations in the first loop and the second loop (e.g. last 4 and 6 in Figure 6 for computing F(1) to F(6)) includes storing butterfly calculation outputs in shuffled order in place of selected inputs to result in a correct ordering of transform outputs (e.g. col. 8 lines 35-48).

Re claim 55, it has same limitations cited in claim 52. Thus, claim 55 is also rejected under the same rationale as cited in the rejection of rejected claim 52.

### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 48-49, 51, 53-54, and 56-57 are rejected under 35 U.S.C. 103(a) as being obvious over Kozaki et al. (U.S. 6,058,409) in view of Aguilar et al. (U.S. 5,473,556).

Re claim 48, Kozaki et al. do not disclose in Figures 6-7 the final stage calculating means performs all butterfly calculations as radix-4 butterflies having four inputs and four outputs. However, Aguilar et al. disclose in Figure 1 an FFT calculation utilizing radix-4 butterflies having four inputs and four outputs (e.g. stage 2). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the

invention is made to add the radix-4 butterflies in FFT as seen in Aguilar et al.'s invention into Kozaki et al.'s invention because it would enable to increase the system performance by reducing the processing time.

Re claim 49, Kozaki et al. further disclose in Figures 6-7 N is a power of two (e.g. 8 samples as  $2^3$  in Figure 6).

Re claim 51, Kozaki et al. do not disclose in Figures 6-7 the non-final and final stage calculating means include a four-fold SIMD processor for performing four radix-4 butterfly calculations at a time. However, Aguilar et al. disclose in Figure 1 four-fold SIMD processor for performing four radix-4 butterfly calculations at a time (e.g. stage 2 wherein four fold of 4-radix is needed for 16 points). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add an four-fold SIMD processor for performing four radix-4 butterfly calculations at a time as seen in Aguilar et al.'s invention into Kozaki et al.'s invention because it would enable to increase the system performance by reducing the processing time.

Re claim 53, it has same limitations cited in claim 48. Thus, claim 53 is also rejected under the same rationale as cited in the rejection of rejected claim 48.

Re claim 54, Kozaki et al. do not disclose in Figures 6-7 storing twiddle factors for application in the butterfly calculations in groups of four, each group having an index and the groups being stored in bit reversed order based on the index. However, Aguilar et al. disclose in Figures 1-2 storing twiddle factors (e.g. Figure 1 for multiplying with data points in stage 2) for application in the butterfly calculations in groups of four, each group having an index and the groups being stored in bit reversed order based on the

index (e.g. Figures 2-3). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a step of storing twiddle factors for application in the butterfly calculations in groups of four, each group having an index and the groups being stored in bit reversed order based on the index as seen in Aguilar et al.'s invention into Kozaki et al.'s invention because it would enable to increase the system performance by reducing the processing time.

Re claim 56, it has same limitations cited in claim 53. Thus, claim 56 is also rejected under the same rationale as cited in the rejection of rejected claim 53.

Re claim 57, it has same limitations cited in claim 54. Thus, claim 57 is also rejected under the same rationale as cited in the rejection of rejected claim 54.

#### ***Allowable Subject Matter***

8. Claim 50 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Response to Amendment***

9. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn. A new art rejection of the Final action is made based on the Amendment filed 08/20/2004.

*Response to Arguments*

10. Applicant's arguments with respect to claims 47-57 have been considered but are moot in view of the new ground(s) of rejection.

*Conclusion*

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 3,673,399 to Hancke et al. disclose a FFT processor with unique addressing.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.



Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do  
Examiner  
Art Unit 2193

June 30, 2005

  
**KAKALI CHAKI**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2100**